

FIG. 3



DDS/PDL

Number of bytes	2 bytes	1 byte	1 byte	//////////////////////////////////////	2 bytes	2 bytes	68 bytes	a 8 bytes	4 bytes	164 bytes	140 bytes				4 bytes	1652 bytes
Contents	DDS identifier (OAOAh)	Reserved	Disc certification flag	#DDS/PDL update counter	Number of Groups	Number of zones	Reserved	Location of Primary spare area	Location of LSN 0	Reserved	Start LSN for Zone 0	Start LSN for Zone 1		Start LSN for Zone 34	DMA rec-counter 1	reserved
ВР	0 to 1	2	က	4 to 7	8 to 9	10 to 11	12 to 79	80 to 87	88 to 91	92 to 255	256 to 259	260 to 263	1 1 1	392 to 395	396 to 399	400 to 2047

F1G. 4

SDL

Contents	Number of bytes
SDL identifier (0002h)	2 bytes
Reserved	2 bytes
SDL update counter	//////////////////////////////////////
Start sector number of Supplementary spare area	4 bytes
Total number of logical sectors	4 bytes
DDS/PDL update counter	4 bytes
Spare area full flags	1 byte
DMA rec-counter 2	4 bytes
Number of entries in SDL	2 bytes
The first SDL entry	8 bytes
	1 1 1
The last SDL entry	8 bytes
Ine last SUL entry	

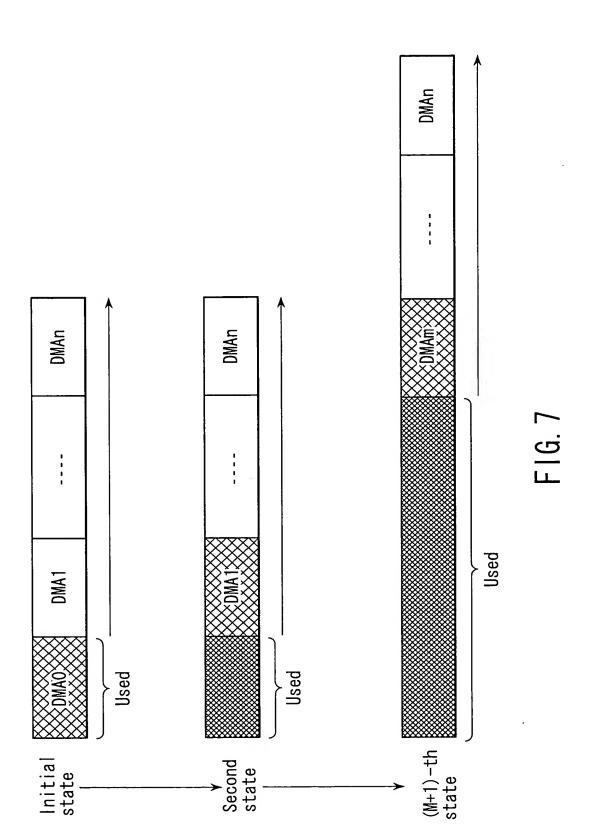
F1G. 5

FIG. 6 RS

PCV (1B)		DCV (1D)	Replacement destination
(a)	address (3B)	(GL) ACV	address (3B)

SDL Entry







## DMA use state 1

	DDS/PDL update counter	SDL update counter	DMA counter
DMA 0	Normal use	Normal use	0~Nov−1
DMA 1	Continuing use of above value	Continuing use of above value	0∼Nov−1
	Continuing use of above value	Continuing use of above value	0~Nov-1
<b>-</b>			
DMA m	Continuing use of above value	Continuing use of above value	0~Nov−1
	Continuing use of above value	Continuing use of above value	0~Nov-1
•			
DMA n	Continuing use of above value	Continuing use of above value	0~Nov−1

Nov:Allowable overwrite count

## F1G. 8



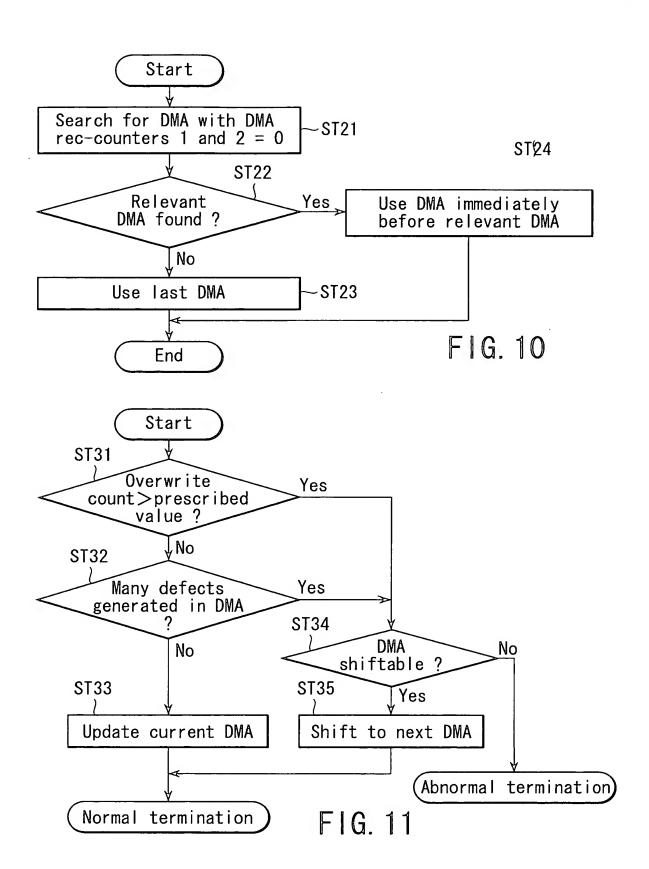
DMA use state 2

	DDS/PDL update counter	SDL update counter	DMA counter
DMA 0	Normal use	Normal use	0~Nov−1
DMA 1	Normal use after reset	Normal use after reset	0~Nov−1
	Normal use after reset	Normal use after reset	0~Nov−1
DMA m	Normal use after reset	Normal use after reset	0~Nov−1
	Normal use after reset	Normal use after reset	0∼Nov-1
DMA n	Normal use after reset	Normal use after reset	1-voV∼0

Nov:Allowable overwrite count

F16.9



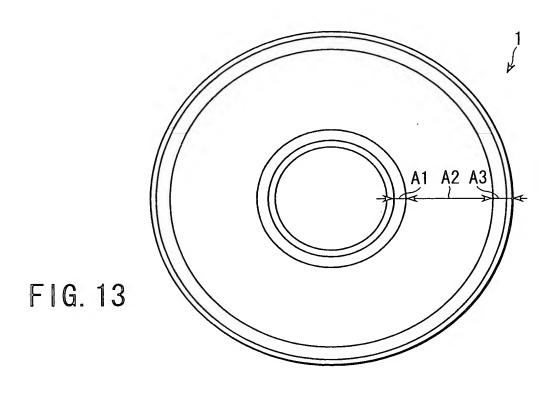


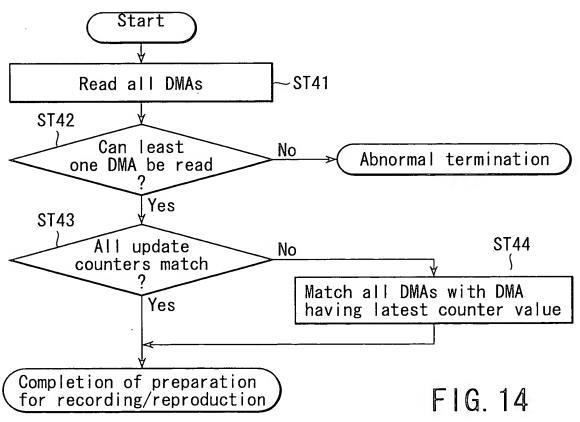
AND O 7 2000 SE

T For innermost	periphery	For	☐ Coutermost ☐ periphery		For junermost	periphery	For	☐ coutermost ☐ periphery		
DMAn	DMAn	DMAn	DMAn	ad in	DMAn	DMAn	DMAn	DMAn		sednences
1	1 1 1	1	1 1 1	Many defects are generated in DMA sequence 3	1 1 1	1 1	1 1	1		Shift to Next DMA in all se
DMA1	DMA1	DMA1	DMA1	Many de DMA seq	SDINA!	<b>∭</b> DMA1	<b>∭</b> DMA1	<b>∭</b> DMA1		Shift to N
DMAO	2 DMAO	3 DIMAO	1 DMAO	ln use		7		1	$\left. \right\}$	ln use
DMA sequence	sequence 2	DMA sequence 3	DMA sequence 4		DMA sequence	DMA sequence 2	DMA sequence 3	DMA sequence 4		
DMA	DMA	γ—	DMA	,	DMA	DMA	DMA	DMA)	r	
	Initial	state			 	* Second	state			

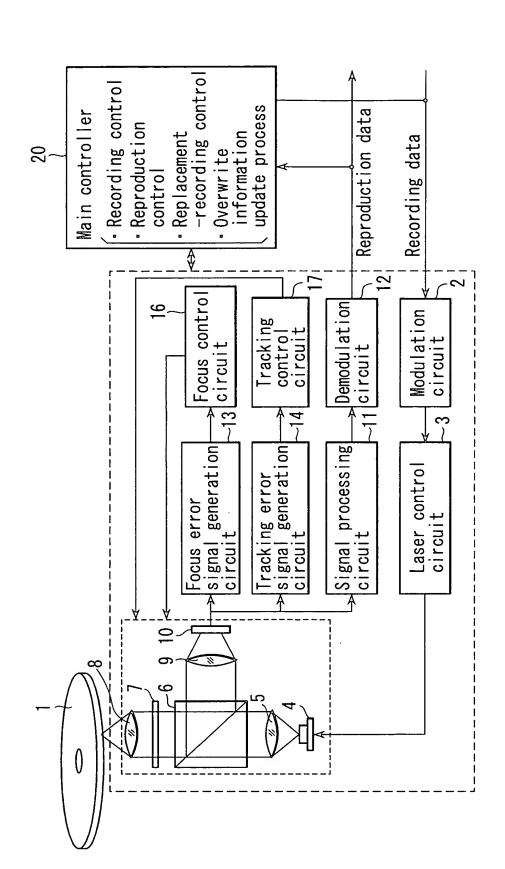
FIG. 12











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FIG. 15